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Application Number 10/714358  
Response to Office Action dated 04/23/2007

**REMARKS**

Applicants request reconsideration of the claims in view of the amendments above and the remarks herein. Applicants amend claims 1 and 19 and add new claim 30; in doing so, Applicants have not added new matter. Support in the originally filed specification for selectively reading from the data buffer is given on page 17, lines 4-5, and page 18, lines 18-22. Support in the originally filed specification for new claim 30 is given in FIG. 1 showing data being simultaneously input into the comparing and determining portion 3 and the data buffer 5 and in FIG. 3 which shows that the step of comparing and determining S202 occurring before the data write process S204; and at page 16, lines 32-36 which states that at the same time the data are evaluated by the comparing and determining portion, the address of the data buffer are updated before the data is written into the data buffer. Claims 1-29 are pending of which claims 4-18 and 20-29 are withdrawn. Applicants address the rejection of claims 1-3 and 19.

**The Rejection of claims 1-3 and 19 under 35 U.S.C. §102(b)**

Applicants respectfully traverse the rejection of claims 1-3 and 19 as being anticipated by PCT WO99/44368, U.S. Patent 6461474 to Hirano et al. (Hirano '474). Hirano '474 does not teach or suggest that "only data having a value that is not 0 (zero) are selectively read out ... from the data buffer" as required by claims 1 and 19. Also, Hirano '474 does not teach or suggest a read control portion of claim 1.

Hirano '474 teaches a method to process image data at high speed wherein consecutive data are written to different memories and then processed. Hirano '474 explicitly teaches that all the data, i.e., data that has both 0 and 1 as the quantized coefficients, are read from the bank memory. Hirano '474 teaches that the data counter determines whether the data supplied by the bank memory is 0, i.e., the data counter counts the number of consecutive 0s and writes a run length representing the number of zeroes, *see* Hirano '474 at column 20, lines 35-36. Thus, all data, even data having a coefficient of 0 are read from the bank memory, contrary to the requirement of claims 1 and 19 that only input data having a value that is not 0 (zero) are selectively read from the

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data buffer. Hirano '474, moreover, teaches that the all data are read from memory and then written into the FIFOs alternatively. So, even if the FIFOs are considered data buffers, then data having coefficients of consecutive 0s are also read from the FIFOs.

It would not be obvious to one of ordinary skill in the art, moreover, to modify Hirano '474 to read only data having a value that is not 0 because Hirano '474 teaches a method of using different alternate memories to process data having a valid portion and an invalid portion, i.e., it is inherent in the teachings of Hirano '474 to require both valid data having a coefficient of 1 and invalid data having a coefficient of 0. Applicants claimed invention of selectively reading data having a value that is not 0 from the data buffer shortens the time that the data buffer is accessed, thus allowing the waiting time before variable-length encoding is performed to be shortened, and allowing the overall speed of encoding to be increased (*see* Applicants' specification at page 5, lines 7-10), even increased beyond that of Hirano '474.

Hirano '474 further does not teach or suggest a read control portion, as required by claim 1. The rejection corresponds the selector 205 and the FIFOs 204a,b as the read control portion. The FIFOs 204 a,b, however, do not selectively read data from the bank memory, the FIFOs 204 a,b acquire data from the data counter portion 203, not from the bank memory 201. Hirano '474 at column 20, lines 30-35, explicitly teaches that "[o]ne of two items of data simultaneously read from the bank memory is transferred to the data counter portion through an 11-bit data bus DB1, and the other is transferred to the data counter portion through an 11-bit data bus DB2." From the data counter portion, the data is transferred to alternate FIFOs. Thus, based on the processing methods set forth by Hirano '474, there is no read control portion because all the data is read.

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Applicants request the Examiner to withdraw the rejection of claims 1-3 and 19 as being anticipated by or obvious in view of Hirano '474. Applicants assert that claims 2, 3 and 30 are allowable at least by virtue of its dependence upon claim 1. Applicants do not concede the correctness of the rejection. Applicants request the Examiner to telephone the attorney, Mr. Douglas P. Mueller, at 612.455.3804 should there remain any impediments to allowance of the claims and issuance of the patent.



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Respectfully submitted,

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